SURFACE TREATED LOW-k DIELECTRIC AS DIFFUSION BARRIER FOR COPPER METALLIZATION

FIELD OF THE INVENTION

[0001] The present invention relates to a method of fabricating a semiconductor device, and more particularly, to an economical method of forming a diffusion barrier for copper (Cu) and/or Cu alloy metallization by modifying the surface properties of the low-k interlayer dielectric layers.

BACKGROUND OF THE INVENTION

[0002] In many high performance, high density semiconductor devices, Cu or Cu alloy is used for the conductive material in the metallization layers. Cu or Cu alloy is generally preferred over aluminum-based metallization in these applications because Cu is a better electrical conductor and is more resistant than aluminum to electromigration. Cu interconnect structures found in these semiconductor devices comprise a substrate, typically doped monocrystalline silicon, and a plurality of sequentially formed low-k interlayer dielectrics and patterned conductive structures formed from Cu (or Cu alloy) based metallization.

[0003] But, because Cu diffuses through the low-k interlayer dielectric materials, the Cu interconnect structures must be encapsulated by a diffusion barrier layer. Otherwise the diffused Cu metal in the low-k interlayer dielectric will result in current leakage between the interconnect structures. The diffusion barrier is typically a metal layer. Typical metal diffusion barrier metals include tantalum, tantalum nitride, titanium, titanium nitride, titanium-tungsten, tungsten, tungsten nitride, titanium silicon nitride, tungsten silicon nitride, tantalum silicon nitride and silicon nitride.

[0004] Shown in Figure 1 is a schematic cross-sectional diagram of a Cu interconnect structure **150** having a conventional diffusion barrier, a Cu capping layer **130**. A Cu interconnect structure **150** and a low-k interlayer dielectric layer **110** are formed on a substrate **100**. The substrate **100** may be any surface, generated when making a semiconductor device, upon which a dielectric layer may be formed. The bottom and sides of the Cu interconnect structure **150** are encapsulated with a barrier layer **120** to prevent Cu from diffusing into the low-k interlayer dielectric **110**. The barrier layer **120** typically comprises a blanket layer of refractory material, such as, tantalum, tantalum nitride, or titanium nitride. The exposed top surface of the Cu interconnect structure **150** is then capped with a diffusion barrier layer **130** of thin silicon nitride

barrier. Generally, another dielectric layer or other type of passivation layer **140** may be deposited on top of the structure shown in Figure 1 and the Cu capping layer **130** prevents Cu from diffusing into the surrounding low-k interlayer dielectric **110**, which could result in electrical short between the Cu interconnect structure **150** and another neighboring Cu interconnect structure **151**. The neighboring Cu interconnect structure **151** is encapsulated with its own set of diffusion barriers **121** and **131.** The capping diffusion barriers **130** and **131** prevent copper diffusion between the metal lines **150** and **151** which would cause unwanted electrical shorts.

[0005] The Cu capping process involves depositing a blanket of a diffusion barrier material, silicon nitride, and then removing the excess material from the top surface of the surrounding interlayer dielectric **110** by chemical-mechanical polishing (CMP). After removing the excess barrier material by CMP, the Cu capping layer **130** remains over the Cu interconnect structure **150**. This conventional method of capping the Cu in damascene process is generally complex and costly and economical alternate process solutions are helpful in reducing the manufacturing costs.

SUMMARY OF THE INVENTION

[0006] According to an aspect of the present invention, a method is disclosed herein for treating the surface of low-k dielectric material to form a diffusion barrier to neighboring copper (Cu) interconnect metal structures in an interconnection structure of a semiconductor device. The method comprises modifying the surface properties of the low-k interlayer dielectric so that the modified surface acts as a diffusion barrier to Cu. This may be achieved by treating the surface of the low-k dielectric with atoms of appropriate material, such as nitrogen or carbon containing medium, to form a thin surface layer of silicon nitride or silicon carbide, respectively, on the low-k dielectric that is chemically inert to Cu. The treatment method may include silicon containing medium when treating an organic based low-k dielectric. The surface treatment can be achieved by techniques, such as, for example, plasma surface treatment, ion implantation, and chemical reaction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The invention will be better understood from the following detailed description of an exemplary embodiment thereof in conjunction with the accompanying drawings in which:

[0008] Figure 1 is a schematic cross-sectional illustration of a prior art Cu damascene structure in which a Cu metallization is capped with silicon nitride layer; and

[0009] Figure 2 is a schematic cross-sectional illustration of a Cu damascene structure at an interim stage before a Cu diffusion barrier is formed on top surface of the low-k interlayer dielectric layer according to an embodiment of the present invention; and

[0010] Figure 3 is a schematic cross-sectional illustration of the Cu damascene structure of Figure 2 after the Cu diffusion barrier has been formed according to an embodiment of the present invention.

[0011] Features shown in the above referenced drawings are not intended to be drawn to scale, nor are they intended to be shown in precise positional relationship.

DETAILED DESCRIPTION OF THE INVENTION

[0012] The method according to an embodiment of the present invention prevents copper diffusion between metal lines eliminates the need for capping a Cu interconnect structure with a diffusion barrier in a semiconductor damascene structure.

[0013] Shown in Figure 2 is a schematic cross-sectional illustration of a Cu damascene structure formed on a substrate **200** depicting two Cu interconnect structures **250a** and **250b** that are illustrative of a plurality of Cu interconnect structures that may be formed on the substrate **200**. After via holes or trenches have been etched into a low-k interlayer dielectric layer **210** and filled with Cu to form the Cu interconnect structures **250a** and **250b**. The process of forming such Cu damascene structure is well known in the art and need not be elaborated here. The side walls and the bottom of the Cu interconnect structures **250a** and **250b** are encapsulated with a diffusion barriers **220a** and **220b**, respectively.

[0014] The substrate **200** may be any surface, generated when making a semiconductor device, upon which a dielectric layer may be formed. The substrate **200** may include, for example, active and passive devices that are formed on a silicon wafer such as transistors, capacitors, resistors, diffused junctions, gate electrodes, local interconnects, etc. The substrate **200** also may include one or more conductive layers that are separated from each other, or from such active and passive devices, by one or more dielectric layers.

[0015] The low-k interlayer dielectric layer **210** is typically silicon based organic-inorganic hybrids, such as, hydrogen silsesquioxane ("HSQ") and methyl silsesquioxane

("MSQ"), etc. The diffusion barrier layers **220a** and **220b** prevent the Cu interconnect structures **250a** and **250b** from diffusing into the low-k interlayer dielectric layer **210**. The diffusion barrier layers **220a** and **220b** may comprise a refractory material, such as tantalum, tantalum nitride, or titanium nitride.

[0016] Figure 3 illustrates the Cu damascene structure of Figure 2 after top surface **212** of the low-k interlayer dielectric **210** has been treated with a method according to an embodiment of the present invention to form a Cu diffusion barrier layer **260**. According to an aspect of the present invention, the top surface **212** of the low-k interlayer dielectric layer **210** is treated by, for example, plasma surface treatment, ion implantation, or chemical reaction. In an embodiment of the present invention, utilizing plasma surface treatment, the top surface **212** of the low-k dielectric layer **210** is bombarded by nitrogen atoms from a plasma formed from nitrogen-containing gases, such as N2 or ammonia. The nitrogen atoms from the plasma will bond with the native silicon atoms in the low-k dielectric material, near the surface of the dielectric, to form a thin layer **260** (less than 100 Å thick) of silicon nitride on the top surface **212** of the low-k interlayer dielectric layer **210**. Silicon nitride is chemically inert to Cu and is a good diffusion barrier to Cu. The silicon nitride layer **260** does not need to be as thick as the deposited Cu capping layers **130** and **131** found in conventional Cu damascene structure illustrated in Figure 1. The silicon nitride layer **260** formed according to the present invention is typically less than 100 angstroms and preferably less than 50 angstroms thick. Because the silicon nitride layer **260** does not need to be as thick as the conventional Cu capping layers, the associated process time is shorter and more economical. Plasma surface treatment process is well known in the art and the process can be readily controlled to achieve a desired thickness of the silicon nitride layer **260**. After the Cu diffusion barrier layer **260** is formed, the whole structure is typically covered with another layer of dielectric or passivation material **240**.

[0017] In another embodiment of the present invention, ion implantation method may be employed using nitrogen-containing gases, such as N2 or ammonia, under high accelerating voltage, about 20-100 keV, to form the silicon nitride layer **260.** The particular accelerating voltage value may be adjusted depending on the particular doping gas used. Again, the details of the ion implantation process need not be discussed here because ion implantation is a well known process and can be readily applied to achieve a desired thickness of the silicon nitride layer **260**.

[0018] In both the plasma surface treatment and the ion implantation embodiments, Carbon-containing gases, such as CO2, may be substituted for the nitrogen containing gases. In which case, the resulting passivation layer will be silicon carbide rather than silicon nitride. Silicon nitride layer is less than 100 angstroms and preferably less than 50 angstroms thick.

[0019] Where the low-k dielectric layers are polymeric dielectrics rather than silicon based dielectrics, the plasma surface treatment of the dielectric can be conducted with silicon containing gas sources along with nitrogen containing gases in the plasma to form a thin silicon nitride layer for passivation. Silicon containing gases such as SiH_4, $Si(CH_3)_4$, and $Si(CH_3)_3H$ may be used.

[0020] In another embodiment of the present invention, a thin layer (less than 100 Å thick) of material that contains silicon and nitrogen may be deposited, for example, by vaporization and then curing the layer to form silicon nitride. The curing may be achieved by baking, E-beam or UV depending on the particular material used. Again, the passivation layer formed on the top surface of the polymeric dielectric is a silicon nitride layer.

[0021] In another embodiment of the present invention, chemicals that contain silicon and nitrogen can be applied to the surface of the low-k interlayer dielectric to form a thin layer of silicon nitride on the surface of the low-k interlayer dielectric through a spontaneous chemical reaction. Silicon and nitrogen contained in the chemicals react at the surface to spontaneously (*i.e.* without any catalysts) form a thin layer of silicon nitride. An elevated temperature, between 50 – 100 deg. C may be needed to enhance the chemical reaction rate. This process does not deposit a layer of film (generally greater than 100 angstroms thick) but the chemicals react with the surface of the low-k dielectric to form a thin layer of silicon nitride for passivation. The thin layer of silicon nitride is, thus, less than 100 angstroms and preferably less than 50 angstroms thick. This embodiment is equally applicable to forming a silicon carbide layer as the passivation layer by using chemicals that contain silicon and carbon.

[0022] It should be noted that the silicon nitride layer that is formed on the surface of the low-k interlayer dielectric according to the present invention is much thinner than the conventional diffusion barrier layer found in conventional dual damascene structures. The silicon nitride layer formed on the top surface of the low-k interlayer dielectric according to the method of the present invention is less than 100 angstroms and preferably less than 50 angstroms thick.

[0023] The method according to the present invention provide more economical way of forming a Cu diffusion layer in processes such as a single or a dual damascene process for forming the Cu interconnect structures in semiconductor devices. It will be obvious to those skilled in the art that the method of the present invention disclosed herein can be applied to other applications where Cu diffusion across a Cu to dielectric interface is a concern.

[0024] While the foregoing invention has been described with reference to the above embodiments, various modifications and changes can be made without departing from the spirit of the invention. For example, other methods or techniques that may be employed to form a thin passivation layer on the surface of low-k dielectric layers by treating the surface of the dielectric are considered to be within the scope of the invention defined by the appended claims.